This listing of claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF CLAIMS:

Claim 1 (Currently Amended) A memory array ~~comprises~~ comprising:

at least one first-type memory device, each of said at least one first-type memory device comprising a first transistor and a first underlying capacitor that are in electrical contact to each other through a first buried strap, said first buried strap positioned on a first collar region; and

at least one second-type memory device, each of said at least one second-type memory device comprising a second transistor and a second underlying capacitor that are in electrical contact to each other through an offset buried strap, said offset buried strap is located at a depth that is different from the depth of the first buried strap, and is positioned on a second collar region, wherein said second collar region including at least said offset buried strap has a length equal to a length of said first collar region including at least said first buried strap.

Claim 2 (Original) The memory array of Claim 1 further comprising:

at least one other-type memory device, each of said at least one other-type memory device comprises another transistor and another underlying capacitor that are in electrical contact to each other through a further-offset buried strap, said further-offset buried strap positioned on another collar region, wherein said another collar region has a length equal to said second collar region and said first collar region.

Claim 3 (Original) The memory array of Claim 1, wherein said first buried strap region and said offset buried strap region are offset by a vertical dimension ranging from about 0.4 μm to about 0.6 μm.

Claim 4 (Original) The memory array of Claim 1, wherein said first underlying capacitor comprises at least one first-bottling region and said second underlying capacitor comprises at least one offset-bottling region.

Claim 5 (Original) The memory array of Claim 1, further comprising a support region.

Claim 6 (Currently Amended) The memory array of Claim 1, wherein said at least one first-type memory device is formed within a first trench[[;]] and said at least one second-type memory ~~cell~~ device is formed within a second trench.

Claim 7 (Currently Amended) The memory array of Claim 6, wherein[[,]] said first trench has a depth ranging from about 1 μm to about 10 μm and said second trench has a depth ranging from about 1 μm to about 10 μm.

Claim 8 (Original) The memory array of Claim 1 wherein a first bottom surface of said first collar region is vertically offset from a second bottom surface of said second collar region.

Claim 9 (Original) The memory array of Claim 8 wherein said first bottom surface is vertically offset from said second bottom surface by a dimension ranging from about 0.4 μm to about 0.6 μm.

Claim 10 (Original) The memory array of Claim 1 wherein said first underlying capacitor and said second underlying capacitor have a vertical orientation.

Claims 11-20 (Cancelled)

Claim 21 (New) A memory array comprises:

at least one first-type memory device, each of said at least one first-type memory device comprising a first transistor and a first underlying capacitor that are in electrical contact to each other through a first buried strap, said first buried strap positioned on a first collar region; and

at least one second-type memory device, each of said at least one second-type memory device comprising a second transistor and a second underlying capacitor that are in electrical contact to each other through an offset buried strap, said offset buried strap positioned on a second collar region, wherein said second collar region has a length equal to a length of said first collar region and wherein a first bottom surface of said first collar region is vertically offset from a second bottom surface of said second collar region.